RECEIVED
CENTRAL FAX CENTER
FEB 1 3 2006

In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Cancelled)

2. (Currently Amended) The TFT-LCD substrate according to claim [[1]] 4, wherein the configuration of the cross-section of the via hole is non-circular shaped.

3. (Currently Amended) The TFT-LCD substrate according to claim [[1]] 4, wherein the via hole is formed by a photolithography process and the pattern of the via hole is determined in accordance with the mask used during the photolithography process.

4. (Currently Amended) ~~The TFT-LCD substrate according to claim 1, further comprising~~ A thin-film transistor liquid crystal display (TFT-LCD) substrate, comprising:

a substrate, which is defined to form a thin-film transistor (TFT) and a contact plug thereon, wherein the source/drain of the TFT is electrically coupled with the contact plug;

a planarization layer, which is disposed on the substrate and comprises a via hole for penetrating the planarization layer to expose to the contact plug, wherein the configuration of the cross-section of the via hole includes a straight edge so that the via hole is formed with a taper at a lateral view by reflow; and

a dielectric material layer deposited at the inner surface of the via hole within the planarization layer and electrically coupled with the contact plug.

5. (Original) The TFT-LCD substrate according to claim 4, wherein the dielectric material layer is made of Indium Tim Oxide (ITO).

6. (Cancelled)

7. (Currently Amended) The TFT-LCD substrate according to claim [[6]] 9, wherein the configuration of the cross-section of the via hole is non-circular shaped.

8. (Currently Amended) The TFT-LCD substrate according to claim [[6]] 9, wherein the via hole is formed by a photolithography process and the pattern of the via hole is determined in accordance with the mask used during the photolithography process.

9. (Currently Amended) ~~The TFT-LCD substrate according to claim 6, further comprising~~ A thin-film transistor liquid crystal display (TFT-LCD) substrate, comprising:

a substrate, which is defined to form a thin-film transistor (TFT) and a contact plug thereon, wherein the source/drain of the TFT is electrically coupled with the contact plug;

a passivation layer, which is deposited on the substrate;

a planarization layer, which is disposed on the passivation layer, wherein the passivation layer and the planarization layer have a via hole for penetrating both the passivation layer and the planarization layer to expose to the contact plug, wherein the configuration of the

cross-section of the via hole includes a straight edge so that the via hole is formed with a taper at a lateral view by reflow; and

a dielectric material layer deposited at the inner surface of the via hole within the planarization layer and electrically coupled with the contact plug.

10. (Original) The TFT-LCD substrate according to claim 9, wherein the dielectric material layer is made of Indium Tim Oxide (ITO).

11. (Cancelled)

12. (Currently Amended) The structure of the via hole within a planarization layer according to claim ~~11~~ 14, wherein the configuration of the cross-section of the via hole is non-circular shaped.

13. (Currently Amended) The structure of the via hole within a planarization layer according to claim ~~11~~ 14, wherein the via hole is formed by a photolithography process and the pattern of the via hole is determined in accordance with the mask used during the photolithography process

14. (Currently Amended) ~~The structure of the via hole within a planarization layer according to claim 11, further comprising~~ A structure of the via hole within a planarization layer, the structure comprising :

a substrate, which is defined to form a thin-film transistor (TFT) and a contact plug thereon, wherein the source/drain of the TFT is electrically coupled with the contact plug;

a planarization layer, which is disposed on the substrate and comprises a via hole for penetrating the planarization layer to expose to the contact plug, wherein the configuration of the cross-section of the via hole includes a straight edge so that the via hole is formed with a taper at a lateral view by reflow; and

a dielectric material layer deposited at the inner surface of the via hole within the planarization layer and electrically coupled with the contact plug.

15. (Currently Amended) The structure of the via hole within a planarization layer according to claim ~~11~~ 14, wherein the structure of the via hole within a planarization layer is applied to a thin-film transistor liquid crystal display (TFT-LCD) substrate.

16. (Cancelled)

17. (Currently Amended) The structure of the via hole within a planarization layer and a passivation layer according to claim ~~16~~ 19, wherein the configuration of the cross-section of the via hole is non-circular shaped.

18. (Currently Amended) The structure of the via hole within a planarization layer and a passivation layer according to claim ~~16~~ 19, wherein the via hole is formed by a photolithography process and the pattern of the via hole is determined in accordance with the mask used during the photolithography process.

19. (Currently Amended) ~~The structure of the via hole within a planarization layer and a passivation layer according to claim 16, further comprising~~ A structure of the via hole within a planarization layer and a passivation layer, the structure comprising:

a substrate, which is defined to form a thin-film transistor (TFT) and a contact plug thereon, wherein the source/drain of the TFT is electrically coupled with the contact plug;

a passivation layer, which is deposited on the substrate;

a planarization layer, which is disposed on the passivation layer, wherein the passivation layer and the planarization layer have a via hole for penetrating both the passivation layer and the planarization layer to expose to the contact plug, wherein the configuration of the cross-section of the via hole includes a straight edge so that the via hole is formed with a taper at a lateral view by reflow; and

a dielectric material layer deposited at the inner surface of the via hole within the planarization layer and electrically coupled with the contact plug.

20. (Currently Amended) The structure of the via hole within a planarization layer and a passivation layer according to claim ~~16~~ 19, wherein the structure of the via hole within a planarization layer and a passivation layer applied to a thin-film transistor liquid crystal display (TFT-LCD) substrate.